Saurabh Tiwari, Senior Principal Engineer

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Date of birth	11 MAY 1976	Nationality	Indian
Place of birth	Raipur, India		

LINKS

LinkedIn

PROFILE

Senior Principal Engineer at Intel Corporation with over 24 years of expertise in computer architecture and software development, driving innovation at Intel Corporation. Proven track record in modelling and simulation, combined with a strong background in SOC performance architecture. Recognised for leadership roles, such as chairing technical committees for prominent industry conferences and holding multiple patents in architecture and performance projection. Committed to advancing artificial intelligence technologies and enhancing SOC architecture through cutting-edge performance analysis.

EMPLOYMENT HISTORY

Mar 2024

Senior Principal Engineer, Intel Corporation

As a Senior Principal Engineer at Intel Corporation, I am focusing on development of Performance, functional simulation models and performance projection tools for Data Center GPU archtiecture to left-shift development of AI software stack.

- Driving innovative methods that enable 100x faster simulation of GPU over traditional transaction-level models. The responsibilities include collaborating with cross-site and cross-functional teams to optimize software for AI and SOC performance architecture.
- Spearheading efforts to develop state-of-the-art simulation solution that has impact across-organizations
- Created and Mentored a high-performance team. Fostering a culture of knowledge sharing and continuous improvement.
- Contributing to the strategic direction of software development methodologies for AI software stack.

Mar 2019 — Mar 2024

Principal AI Software Engineer, Intel Corporation

Led development and implementation of advanced software solutions for modeling of AI ASIC inference product for Facebook as primary customer.

- This position required a deep understanding of chip development process, software development for AI stack, and verification methodologies and impacting them all with an in-house modeling environment created spefically for the purpose of keeping design and software in-sync.
- Collaboration with hardware teams to ensure software-hardware integration was a key component of the role. Continual assessment of software performance and optimization strategies were vital in enhancing the overall system architecture.
- Collaborated with interdisciplinary teams to ensure seamless integration of software with hardware components. - Conducted extensive performance testing and optimization to meet stringent project requirements.
- Published multiple papers and a patent on advancements done in the role

Mar 2013 — Mar 2019

Technical Manager and Lead modeling architect, Intel Corporation

Created a team and infrastructure for AI ASIC modeling.

- Architecture simulation solution based on System C industry-standard framework, used for simulation of accelerator products, and Imaging IP.
- Expert in pre-silicon Performance-Validation methodologies development, including micro-benchmark and performance-correlation tools.
- Managing team of Performance Architects, Simulation and Modeling Engineers working on On-die interconnect, Cache, Memory and IP integration.

Feb 2004 — Mar 2013

SOC Performance Architect, Intel Corporation

Developed simulation infrastructure for SOC performance modeling, based on SystemC transaction level modeling methodology. Created performance models for on-die cache, interconnect, and DRAM memory controllers connected to CPU and GPUs for client microprocessors at Intel. Successfully delivered 3-4 generations of mainstream CPU SOCs with improvements in performance per generation

Jan 2000 — Feb 2004

Senior Software Engineer, Texas Instruments

Worked on Texas Instruments mainstream mobile Digital Signal Processing (DSP) cores performance model development. The role involved developing instruction set simulator and working closely with architecture, hardware-verification team and kernels development teams. One of key accomplishment of my role was developing a new mode about 100x faster than existing instruction set simulator of the DSP core.

EDUCATION

Jul 1998 — Jan 2000

Master of Engineering, Indian Institute of Science (IISc), Bangalore

Jul 1994 — Jun 1998

Electronics and Communication Engineering, National Institute of Technology, Raipur

SKILLS

C++	Expert	System Architecture	Expert
Software Development	Expert	Cross-Functional Collaboration	Expert
Performance Analysis	Expert	Technical Leadership	Expert
Artificial Intelligence	Skillful		